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EXAMINER	
IQBAL, NADEEM	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 10/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,843	ABDO, AYMAN G.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 5-26* is/are rejected.

7)☒ Claim(s) *2-4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 24 is missing, thus effecting the numbering of claims. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5, 6, & 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Fischer et al., (U.S. Patent number 6,732,311).

1. As per claims 1 & 7, Fischer et al., teaches (col. 4, lines 16-19) an integrated circuit 10, having a debugger 16, the integrated circuit comprises a processor block 12, that includes two cores. He thus teaches limitations pertain to an apparatus comprising a test controller, coupled between a bus and first and second cores in a multi-core computer. He also teaches a memory 14, an instruction register 160 (Fig. 1). He also teaches (col. 4, lines 26-28) that the debugger may insert debugging instructions to be performed by the core. He thus teaches limitations pertain to operating a data flow stress test in the multi-core computer.

3. As per claim 5, He also teaches (Fig. 1, col. 6, lines 50-53) that the multiplexer 166 will return to passing normal instructions from memory block 14 after a return instruction, indicating that debugging is complete. He thus teaches electrical deactivation of the debugger after the test.

4. As per claim 6, He teaches (col. 4, lines 16-19) an integrated circuit 10, having a debugger 16, the integrated circuit comprises a processor block 12, that includes two cores. He thus teaches the test controller, first core, and the second core are all disposed on a same integrated circuit.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al., (U.S. Patent number 6,732,311).

3. As per claim 8, Fischer et al., teaches (col. 6, lines 6-8) a multiplexer 166 that is used to control the flow of data and instructions to the processor block 12. He also teaches (col. 4, lines 40-42) a multiplexer 124 serves as a gate to allow a selected core to exchange information with memory block 14. He does not explicitly discloses the switching logic to switch the bus between data request from at least one of the first and second cores and test data requests. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to realize that he includes the switching logic since he teaches the multiplexers 166 and multiplexer 124,

that performs the equivalent functionality of the claimed switching logic by allowing a selected core to exchange information with memory block 14, and to control the data flow and instructions.

4. As per claim 9, He teaches (col. 6, lines 10-12) an instruction register 160 that hold test instructions.

6. As per claim 10, He also teaches (Fig. 1, col. 6, lines 50-53) that the multiplexer 166 will return to passing normal instructions from memory block 14 after a return instruction, indicating that debugging is complete. He thus teaches electrical deactivation of the debugger after the test.

7. As per claim 11, He teaches (col. 4, lines 16-19) an integrated circuit 10, having a debugger 16, the integrated circuit comprises a processor block 12, that includes two cores. He thus teaches the test controller, first core, and the second core are all disposed on a same integrated circuit.

5. As per claim 12, Fischer teaches (col. 6, lines 14-16) a debugging initiating instruction from instruction register will prompt a core to point to debugging instructions stored at a memory address in memory block 14. He thus clearly provides to block a data request from a first core to a bus and send instead a debugging initiating instruction.

6. As per claim 13, He teaches (col. 6, lines 14-16) a debugging initiating instruction from instruction register will prompt a core to point to debugging instructions stored at a memory address in memory block 14. He therefore would also send a second data request from a second core to the bus.

7. As per claim 14, He teaches (col. 6, lines 32-35) that if a debug signal is received by multiplexer 166 from debug FSM 165, multiplexer 166 will continue to pass data from memory

block 14 to processor block 12 while substituting instructions from instruction register 160. FSM is part of the test controller (debugger), therefore the debugger controls the blocking and the sending of instructions.

8. As per claim 15, He teaches as stated above a debugging initiating instruction from instruction register will prompt a core to point to debugging instructions stored at a memory address in memory block 14. He therefore teaches a register that selects the test data request.

9. As per claim 16, He already teaches as stated above a debug signal received by multiplexer 166 from debug FSM 165, multiplexer 166 will continue to pass data from memory block 14 to processor block 12 while substituting instructions from instruction register 160. He thus would provide blocking a second data request from a second core to the bus.

10. As per claim 17, Fischer substantially teaches the claimed invention as disclosed related to claim 12 above. He also teaches (col. 6, lines 14-16) a debugging initiating instruction from instruction register will prompt a core to point to debugging instructions stored at a memory address in memory block 14. He thus clearly provides to block a data request from a first core to a bus and send instead a debugging initiating instruction.

11. As per claim 18, He teaches (col. 6, lines 14-16) a debugging initiating instruction from instruction register will prompt a core to point to debugging instructions stored at a memory address in memory block 14. He therefore would also send a second data request from a second core to the bus.

12. As per claim 19, He teaches (col. 6, lines 32-35) that if a debug signal is received by multiplexer 166 from debug FSM 165, multiplexer 166 will continue to pass data from memory block 14 to processor block 12 while substituting instructions from instruction register 160. FSM

is part of the test controller (debugger), therefore the debugger controls the blocking and the sending of instructions.

13. As per claim 20, He teaches as stated above a debugging initiating instruction from instruction register will prompt a core to point to debugging instructions stored at a memory address in memory block 14. He therefore teaches a register that selects the test data request.

14. As per claim 21, He already teaches as stated above a debug signal received by multiplexer 166 from debug FSM 165, multiplexer 166 will continue to pass data from memory block 14 to processor block 12 while substituting instructions from instruction register 160. He thus would provide blocking a second data request from a second core to the bus.

8. Claims 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al., (U.S. Patent number 6,732,311) in view of Miner et al., (U.S. Patent number 6,732,311).

15. As per claim 22, Fischer teaches (col. 6, lines 14-16) a debugging initiating instruction from instruction register will prompt a core to point to debugging instructions stored at a memory address in memory block 14. He thus teaches limitations pertain to obtain test data for stress testing a multi-core computer system. He also teaches (col. 3, lines 40-43) s status vector register for storing one or more status events, a comparator for comparing one or more status events with internal integrated circuit signals to generate an indicator at its output in the event of a match. He thus teaches limitations pertain to reading a test result from the test register. provides to block a data request from a first core to a bus and send instead a debugging initiating instruction. He does not explicitly discloses writing the test data to a test register in the multi-core computer system through a test port. Miner teaches (page 1, section 0019, lines 2-4) a test access port that may be used as an access mechanism to implement test modes. It would have

been obvious to a person of ordinary skill in the art to include the test access port of the type taught by Miner into the invention of Fisher since it provides an access mechanism to implement test modes, thus allowing writing test data to a test register. Miner also teaches that the access port (TAP) facilitate testing of an integrated circuit, thus provides motivation for the stated inclusion.

16. As per claim 23, Miner teaches (page 2, section 0022, lines 1-3) that the TAP interface may be utilized to allow test instructions and associated test data to be fed into a component and may allow results of execution to be read out of the component. The stated inclusion therefore would allow writing an 'on' bit to the test register.

17. As per claim 25, Fischer teaches (col. 4, lines 10-12) a controller that monitors and controls the system including performing test and diagnostic functions, initializing and housekeeping tasks, therefore would write specifying data requests to be monitored.

18. As per claim 26, Miner teaches as stated above that the TAP interface may be utilized to allow test instructions and associated test data to be fed into a component and may allow results of execution to be read out of the component. He thus allows the ability to write to specify test data requests.

Allowable Subject Matter

19. Claims 2-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (571) 272-3659. Examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703)-305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nadeem Iqbal
Primary Examiner
Art Unit 2114

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